a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode to said second gate electrode.

Claim 8 (amended). The ferroelectric transistor according to claim 1, comprising an auxiliary layer disposed between said ferroelectric layer and said first gate electrode.

Claim 11(amended). A memory cell configuration including a plurality of memory cells, each one of said plurality of said memory cells including a ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

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a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode to said second gate electrode.